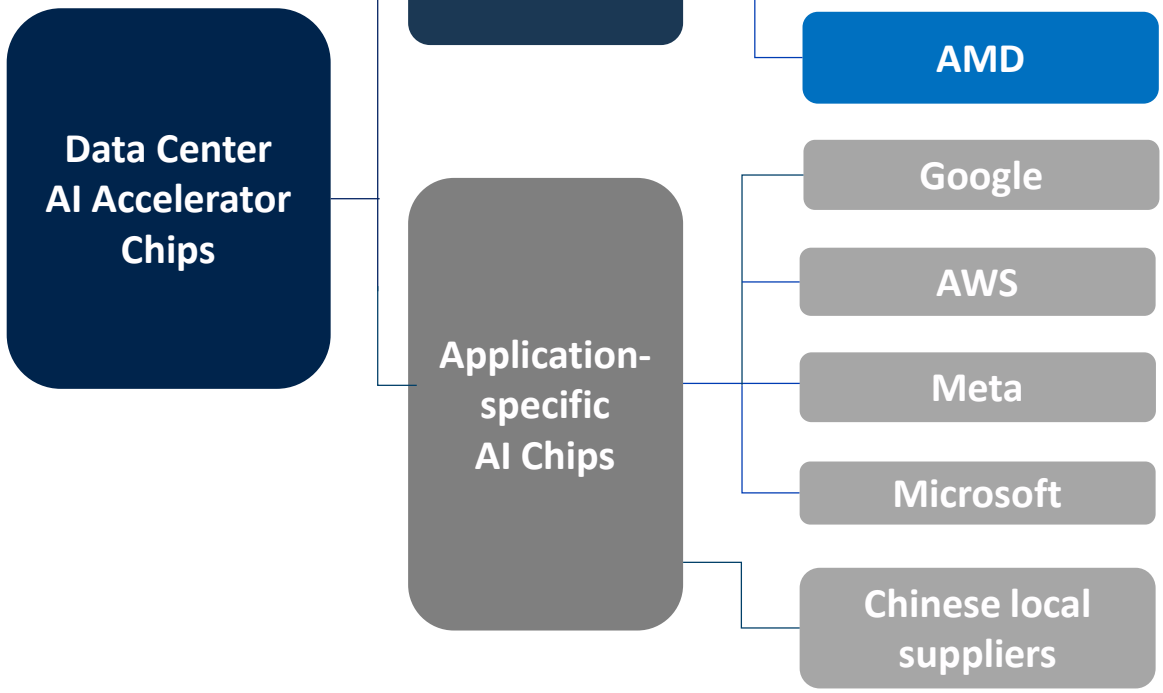
DIGITIMES asia

Global Data Center AI Chip Packaging Market Forecast 2024-2030

Unlocking Fast-Growing Opportunities in AI Wave

Contents

Definition: Data Center AI Chips – AI Accelerators



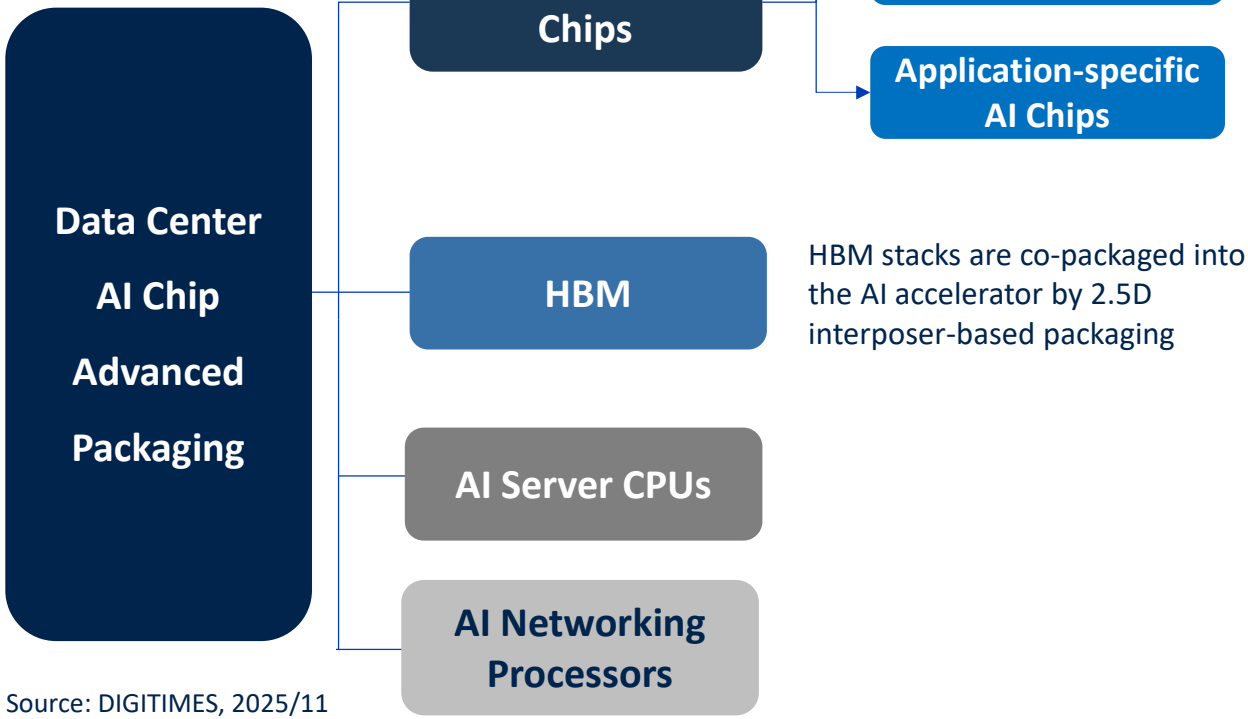
Representative chips in roadmaps

- Hopper architecture GPUs: H100/H200, and H20
- Blackwell architecture GPUs: B100/B200/B300
- Rubin architecture GPUs: R200/R300/ CPX
- Feynman architecture GPUs
- MI250/MI300/MI325/MI400
- Google's TPU V1~V8
- Trainium 2~4; Inferentia 1,2
- MTIA-T 1.0, 1.5.2, 3
- MTIA-I 1.0, 2.0, 3.0, 4.0
- Maia 100, 200
- Huawei's Ascend 910A/910B/910C/…960
- Cambricon's AI chips

Note： GPUs stand for general-purpose GPUs, and application-specific AI chips include AI ASICs and AI ASSPs.

Source: DIGITIMES, 2025/11

Definition: Data Center AI Chip Advanced Packaging



HBM stacks are co-packaged into the AI accelerator by 2.5D interposer-based packaging

Representative packaging technologies

- CoWoS, FoCoS-Bridge, FOEB, Foveros
- System on Wafer (SoW)
- SoIC, Foveros Direct, X-Cube

- CoWoS, FoCoS-Bridge, FOEB, Foveros
- SoW
- SoIC, Foveros Direct, X-Cube

- Micro-bump TCB (Thermo-Compression Bonding)
- Hybrid Bonding (2028~)

- CoWoS, FoCoS-Bridge, Foveros, EMIB
- Foveros Direct
- Not including 2D Fan-outs and traditional FC-BGA packaging.

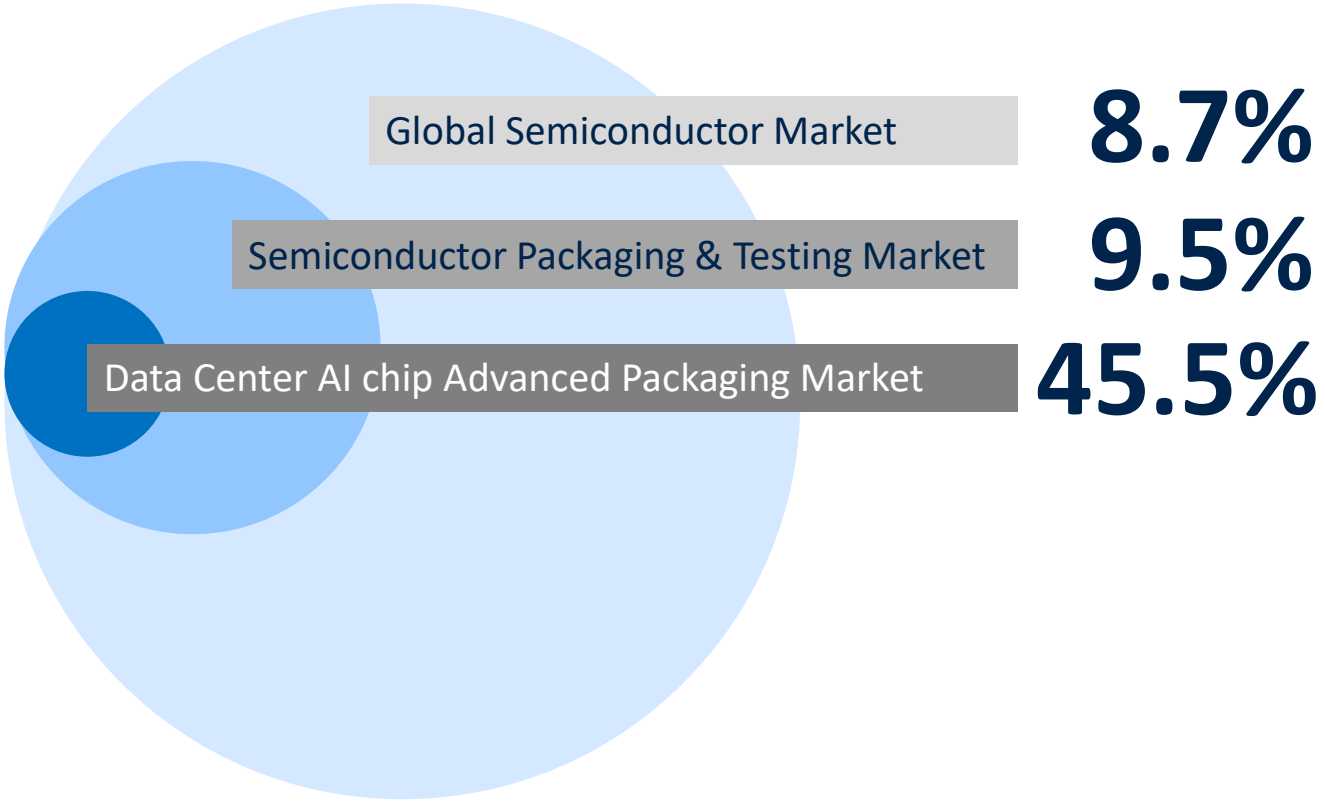
- CoWoS and similar technologies
- 2.5D Fan-out for Co-Packaged Optics (CPO)
- SoIC for EIC/PIC integration in optical engines(OE)

Source: DIGITIMES, 2025/11

- In the following pages, the term “custom AI chips” is equivalent to “application-specific AI chips,” and “GPU” is equivalent to “GPGPU”.
- AI networking processors consist of Switch ICs, DPUs/SmartNICs, and custom AI rack-scale-up interconnect chips for NVSwitch/UALink and similar AI networking technologies within the rack.

Executive Summary (1): Data Center AI Chip Advanced Packaging Growth Strongly Outpacing the Semiconductor Market

2024–2030 Growth Comparison: Semiconductor, Packaging & Testing, and AI Chip Advanced Packaging



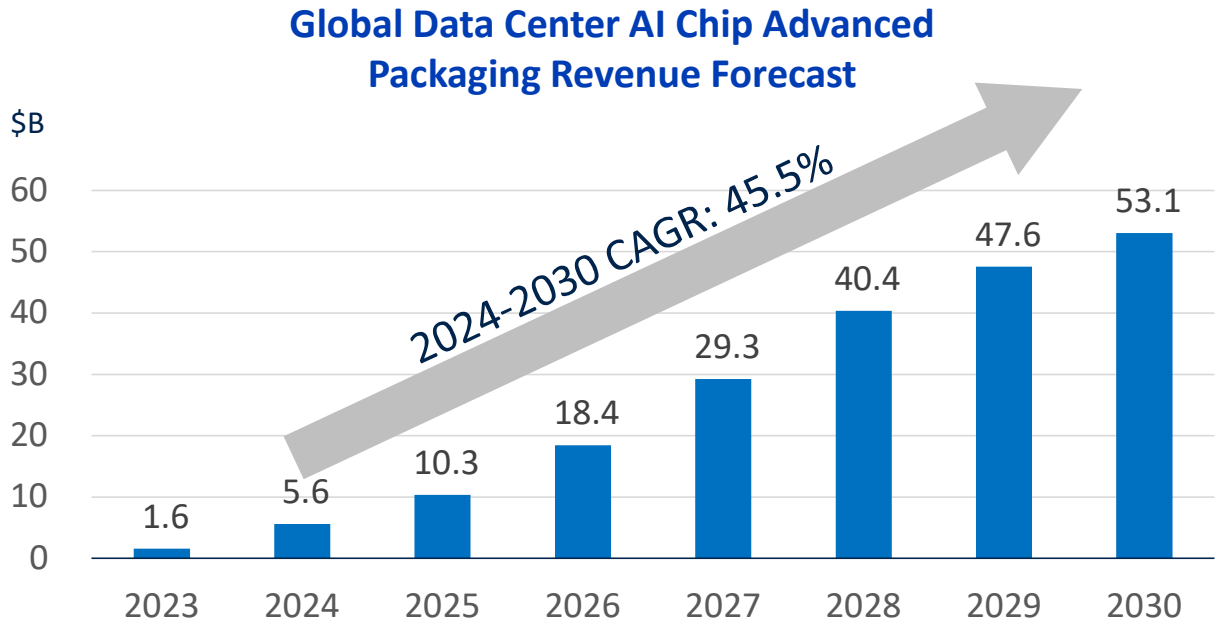
- With the generative AI surge, the global semiconductor market is set to exceed US$1 trillion by 2030, growing at an 8.7% CAGR from 2024–2030.
- The overall packaging and testing segment is growing faster at a 9.5% CAGR over the same timeframe.
- Crucially, the datacenter AI chip advanced packaging market is poised for explosive growth, featuring an impressive 45.5% CAGR through 2030.

[5]Source: DIGITIMES, 2025/11

Executive Summary (2): Datacenter AI Advanced Packaging to Hit $53.1B, Driven by CoWoS and other 2.5D/3D Technologies

Global data center AI chip advanced packaging revenue increases from $5.6B in 2024 to $53.1B in 2030, with a 45.5% CAGR.

- Data center AI chip advanced packaging includes 2.5D CoWoS, 3D SoIC, SoW, and similar packaging technologies for AI accelerators, AI server CPUs, HBM, and AI networking.
- CoWoS (Chip-on-Wafer-on-Substrate)/CoPoS (Chip-on-Panel-on-Substrate) and similar technologies are expected to account for 58% of the market by 2030.
- System on Wafer(SoW) and SoIC-like 3D stacking will gain market share from CoWoS.

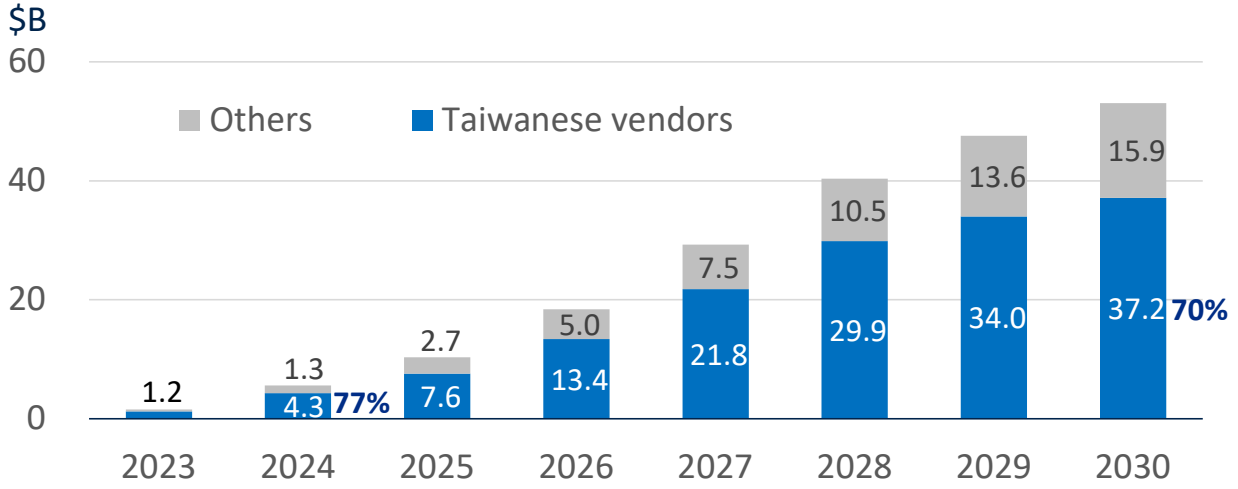


Source: DIGITIMES, 2025/11

Executive Summary (3):Taiwanese players will continue to hold over 70% of the data center AI chip packaging market by 2030

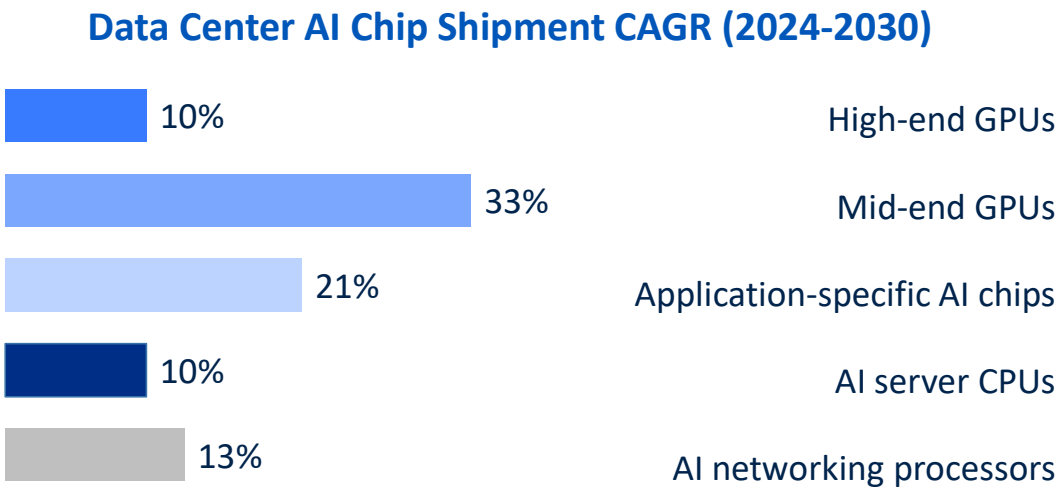
- **Taiwan's share of global data-center AI chip packaging is projected to moderately decline from 77% in 2024 to 70% by 2030, indicating increasing competition from other regions.**
  - Intel, Samsung, and Rapidus are all working on their own advanced packaging technologies.
  - Amkor and other companies, such as those from Singapore and Malaysia, will increase their investments in advanced packaging.
  - China's self-sufficiency policy will boost the growth of Chinese local companies in the advanced packaging sector.
- **Why can Taiwanese vendors still hold a 70% market share by 2030?**
  - TSMC is the leader in advanced wafer fabrication and in various 2.5D/3D packaging technologies.
  - Besides TSMC, Taiwan has a highly competitive AI rack and semiconductor supply chain that collaborates closely with leading hyperscalers and leading chip platform vendors.

Taiwanese Vendors' Data Center AI Chip Advanced Packaging Revenue Forecast



Source: DIGITIMES, 2025/11

Application-specific AI Chip Shipments CAGR by 21% from 2024 to 2030, Surpassing the growth of AI GPUs and CPUs



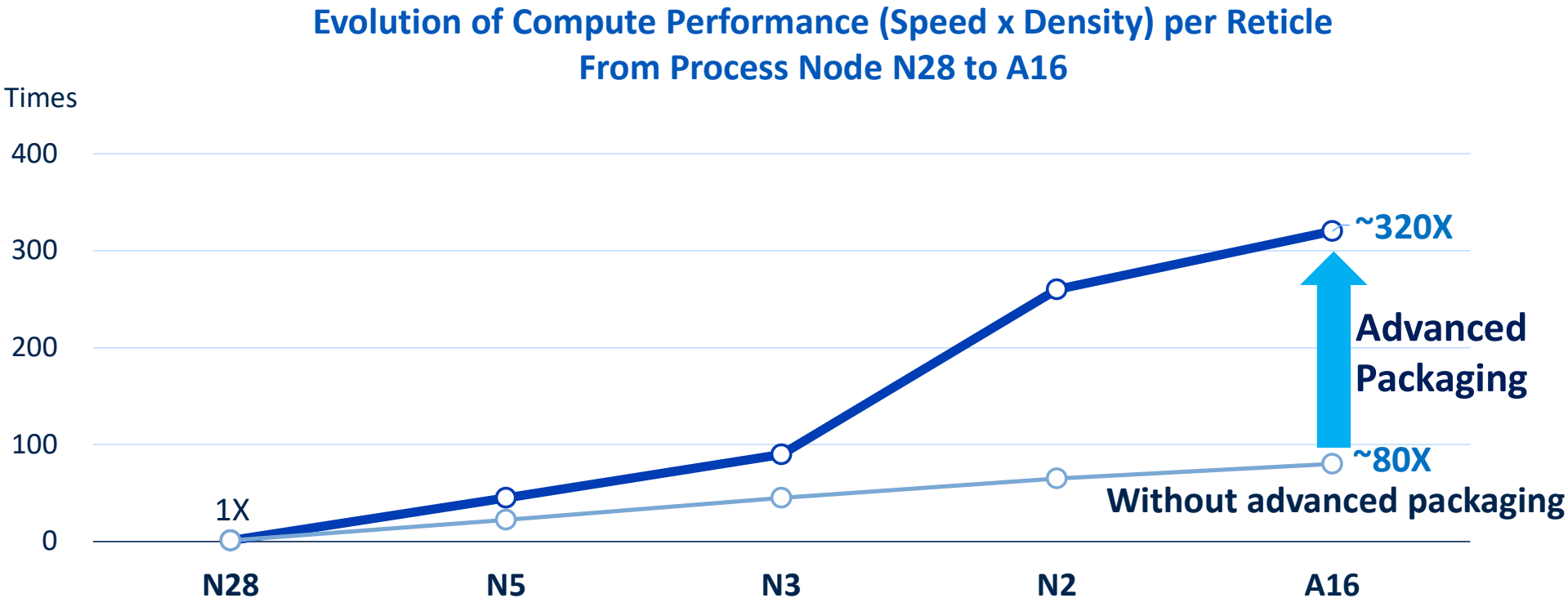
Total GPU advanced packaging revenue is projected to exceed 1.4 times that of application-specific AI chips by 2030.

Source: DIGITIMES, 2025/11

- **The mid-end GPUs will grow fastest due to their low base in 2024. On the other hand, High-end GPUs have the lowest CAGR (9.9%) due to their high base in 2024 and the increase in dies per chip in the coming years. It is worth noting that high-end GPUs will remain the largest segment of the AI chip market in terms of foundry revenue by 2030, mainly due to their large chip sizes and adoption of advanced process technologies.**
- **The CAGR of application-specific AI chips will be higher than that of GPUs.**
  - The shipment of Google TPUs will increase significantly for internal use and for external GCP customers such as Apple, OpenAI, and Anthropic.
  - The catch-up of Chinese vendors like Huawei and Cambricon to support China's self-sufficiency policy.
- **AI server CPU shipments CAGR is expected to grow (10%) because the demand for GPUs and application-specific AI chips is much higher than that for CPUs.**
- **AI networking chips have a 13% CAGR, but only high-end switch chips require CoWoS or other 2.5D packaging to reduce the path length for large switch dies and HBM.**

Advanced Packaging Improves Performance Significantly

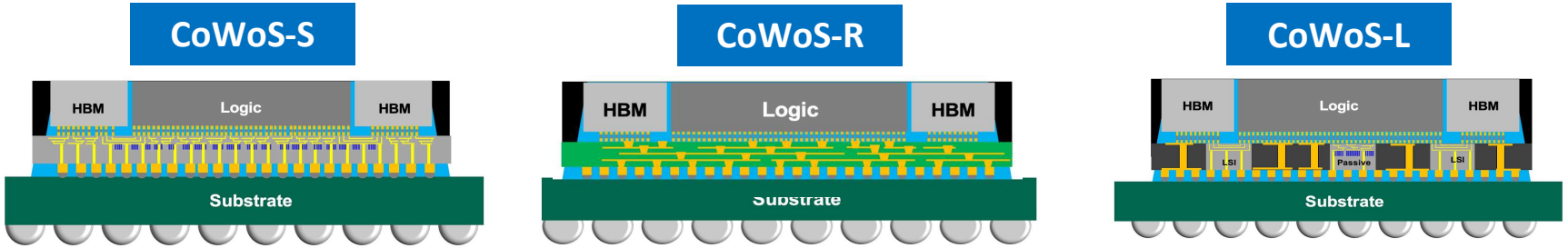
- Without advanced packaging, compute performance per reticle area would increase by 80X (purely due to process-node improvements) from N28 to A16.
- Combined with advanced packaging, the compute performance of the A16 process node achieves a 320X improvement over the N28 node.



Source: TSMC, 2025/9

CoWoS-L Combines the Benefits of CoWoS-S and CoWoS-R, Offering High Performance and Large Interposer Availability

Comparison of CoWoS Family



Source: TSMC, 2023

	CoWoS-S	CoWoS-R	CoWoS-L
Interposer material	Silicon	Redistribution Layers (RDL)	Silicon Bridge + RDL
Interposer size	1~3.3X reticle size	1.4~5.5X	3X ~ >9X
# of HBM Stacks	8	8/12	8/12/16
Performance	good	medium	good
Cost	high	Lower than CoWoS-S	Initially highest for complexity
Applications	AI accelerators; FPGA for data center and networking	AI accelerators; AI networking ICs; (suitable for cost-concerned and large interposer applications)	AI/HPC: especially suitable for large interposers to attach more big dies and multiple HBM stacks.
Customers	Nvidia, AMD, Google…	AWS	First customer: Nvidia (Blackwell)

Source: DIGITIMES, 2025/11

- CoWoS-L and CoWoS-R are the solutions for larger interposers, CoWoS-L can also provide near the CoWoS-S performance in finer pitch applications.

Appendix

OUR TEAM


OUR TEAM
Co-Researcher
Eric Huang
Vice President
#Semiconductor
Co-Researcher
Tony Huang
Director
#Semiconductor & Display

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研究報告	到府簡報	系列論壇	Special Report	顧問專案
研究報告涵蓋七大領域23個頻道與全球產業數據，每年發佈超過300篇報告，內容以分析全球及台灣產銷狀況、產業發展現況、產品技術趨勢、領導廠商策略及競爭態勢。包括區域及新興市場研究和關鍵零組件發展，即時提供客戶所需的產業情報，為台灣最專業且權威的產業分析服務。	以九大分類提供宏觀大勢/供應鏈布局、半導體、Display Trends通訊產業趨勢/5G/B5G/、垂直應用/專網/O-RAN、NB/高效能運算(HPC)/Cloud、EV/未來車、AI、物聯網(IoT)、智慧應用/數位轉型等領域的研究報告為基礎，整合當前產業發展熱門議題，提供企業專屬的到府簡報服務。	以科技大勢為焦點的系列論壇，每年精心策劃四場圍繞當前熱門議題的精彩活動，探討最新科技趨勢與創新應用，此外，還有一場年度重磅論壇，科技大勢展望未來，解析未來科技發展方向與潛在機遇，幫助企業掌握先機，提升競爭力。論壇旨在促進科技與產業的深度融合，推動創新發展，共同迎接科技新時代的挑戰和機遇。	每年推出四篇長篇報告，深入分析當前焦點產業，提供全面的產業脈絡、市場動態及技術演進。報告旨在為企業領袖、投資者和從業者提供權威的資訊和深刻的洞察，幫助他們掌握產業趨勢，做出明智決策。通過詳細的數據分析和專業見解，助企業在快速變化的市場中保持競爭優勢，洞悉未來發展機遇，驅動創新和增長。	根據企業的研究需求，訂定專屬研究範疇，提供量身定制的研究服務。專注於資訊、消費性電子、通訊、半導體、汽車科技、人工智慧、物聯網、平面顯示器等領域。以深入的產業分析和專業見解，助力企業洞悉市場趨勢，制定精確策略，在快速變化的科技環境中抓住機遇，實現創新和提升競爭力。

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